

Figure 1A

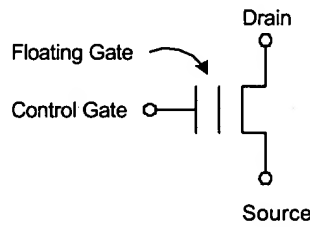


Figure 1B

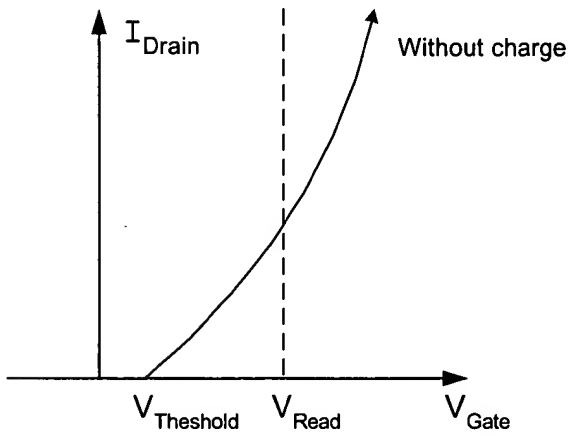


Figure 1C

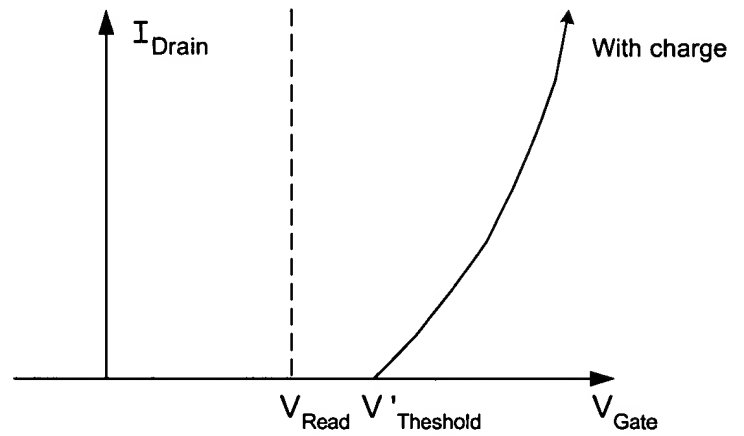


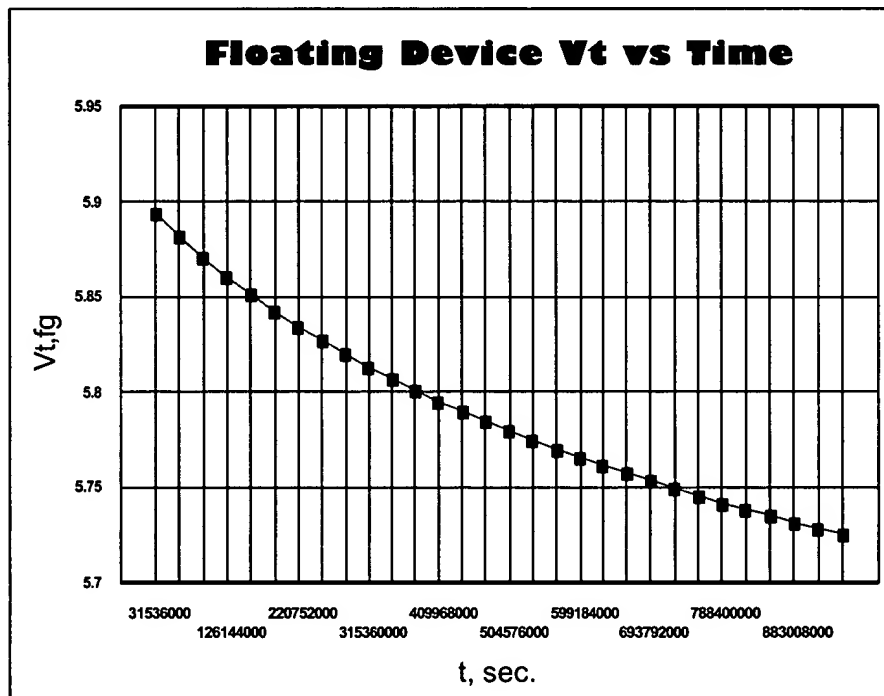
Figure 1D

Calculation of nvm memory cell retention characteristics

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	31536000	1 year
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.054588E-034	94608000	3 years
					1.89E+008	6 years
b0, eV (barrier)	el	mr, effective mass ratio	T, K degree		2.84E+017	9 years
2.9	3.9	0.5	300		3.78E+008	12 years
					4.73E+008	15 years
C	b				9.08E+009	18 years
1.0630E-006	2.3854E+008				6.62E+008	21 years
					7.57E+008	24 years
					8.51E+008	27 years
					9.46E+008	30 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrux um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1078	Capacitance between the floating gate and the drain
Cfs fF	0.7547	Capacitance between the floating gate and the source
Cfg fF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating charged voltage
Va	0.00	Actual erase voltage (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.907
31536000	5.894
63072000	5.882
94608000	5.871
1.26E+008	5.861
1.58E+008	5.852
1.89E+008	5.843
2.21E+008	5.835
2.52E+008	5.827
2.84E+008	5.820
3.15E+008	5.814
3.47E+008	5.807
3.78E+008	5.801
4.1E+008	5.795
4.42E+008	5.790
4.73E+008	5.785
5.05E+008	5.780
5.36E+008	5.775
5.68E+008	5.770
5.99E+008	5.766
6.31E+008	5.762
6.62E+008	5.757
6.94E+008	5.753
7.25E+008	5.750
7.57E+008	5.746
7.88E+008	5.742
8.2E+008	5.739
8.51E+008	5.735
8.83E+008	5.732
9.15E+008	5.729
9.46E+008	5.726



Figures 1E-1F

Calculation of non memory cell retention characteristics

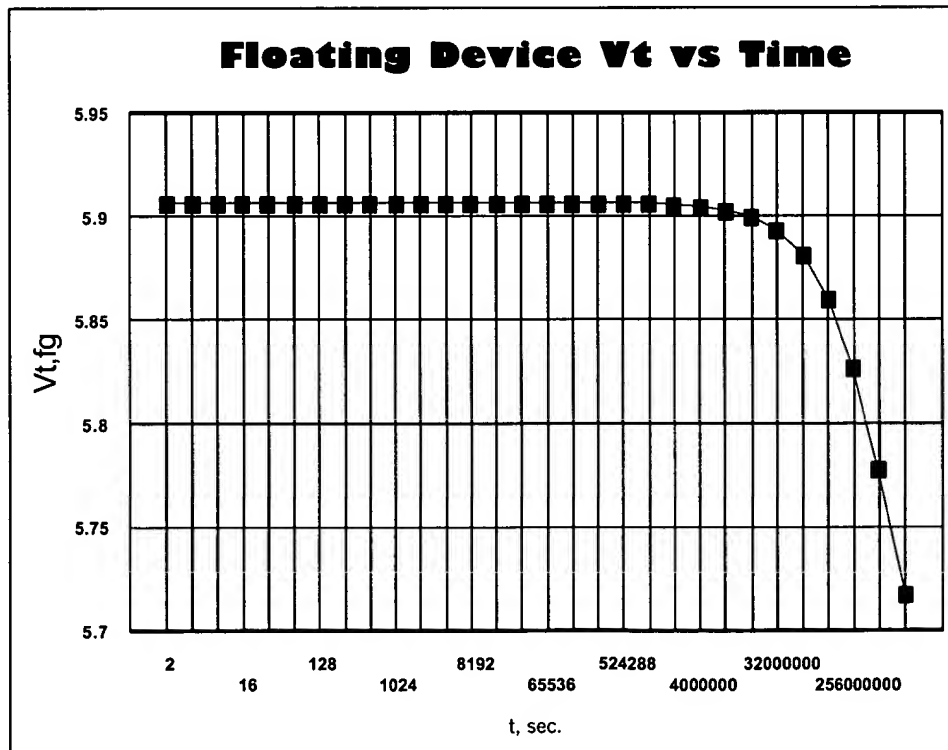
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	Seconds	Time Period
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	60	1 minute
					3600	1 hour
					86400	1 day
					604800	1 week
					2592000	1 month
					1 year
					4 years
					16 years
					32 years

C 1.0630E-006
b 2.3854E+008

Lfg um 0.6000 Channel length of floating gate device
Wfg um 1000.0000 Channel width of floating gate device.
Hfg um 0.0900 Thickness of floating gate polysilicon conductor
Wrx um 0.5000 Width of floating gate overlapping shallow trench isolation
Ttunox A 80 Tunnel oxide thickness
Tono A 190 Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A 300 Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um 0.0500 Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um 0.3500 Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2 0.0438 Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF 1089.5358 Capacitance between the floating gate and the control gate
Cfsx fF 0.4313 Capacitance between the floating gate and the silicon substrate
Cfd fF 0.1078 Capacitance between the floating gate and the drain
Cfs fF 0.7547 Capacitance between the floating gate and the source
Cfg fF 1090.8295 Total floating gate capacitance
Cr,wl 0.9988 Control gate to floating gate coupling ratio
Cr,src 0.0007 Source junction to floating gate coupling ratio

Vt,fg V 0.90 Threshold voltage of floating gate MOSFET
Verase 0.00 Erase voltage applied to the source(not used here, set to zero)
Vfg,ini -5.00 Initial floating charged voltage
Va 0.00 Actual erase volatge (equal to applied + charge stored on the floating)
S 3.76E+016 Derived parameter in the floating gate "erase" equation
X 1.27E+011 Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.906
4000000	5.905
8000000	5.904
16000000	5.900
32000000	5.894
64000000	5.881
.....	5.860
.....	5.827
.....	5.779
.....	5.718



Figures 1G-1H

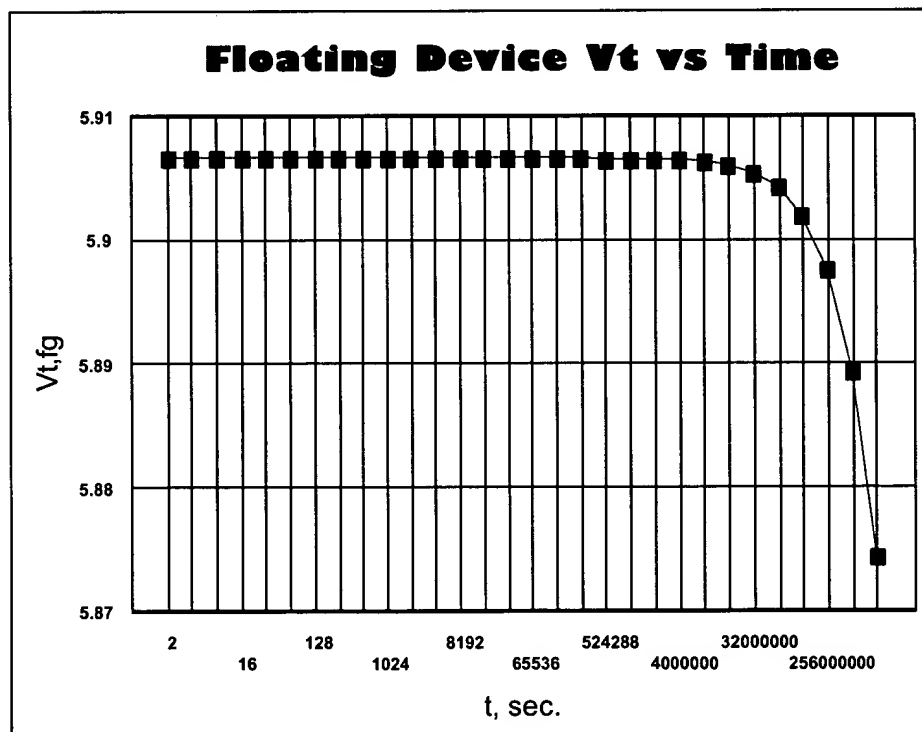
Calculation of nvm memory cell retention characteristics

q_0 , C 1.6022E-019 m_0 , kg 9.1095E-031 k_b , J/K 1.38062E-023 h , J-s 6.62617E-034 h_b , J-s
 b_0 , eV (barrier) ϵ_l 2.9 m_r , effective mass ratio 3.9 T , K degree 300
 C 1.0630E-006 b 2.3854E+008

Seconds Time Period
 60 1 minute
 3600 1 hour
 86400 1 day
 604800 1 week
 2592000 1 month
 1 year
 4 years
 16 years
 32 years

L_{fg} μm 0.6000 Channel length of floating gate device
 W_{fg} μm 1000.0000 Channel width of floating gate device.
 H_{fg} μm 0.0900 Thickness of floating gate polysilicon conductor
 W_{rx} μm 0.5000 Width of floating gate overlapping shallow trench isolation
 T_{tunox} A 85 Tunnel oxide thickness
 T_{ono} A 190 Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
 T_{swox} A 300 Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
 X_{fd} μm 0.0500 Length of floating gate overlapping drain region of the floating gate MOSFET
 X_{fs} μm 0.3500 Length of floating gate overlapping source region of the floating gate MOSFET
 A_{inj} μm^2 0.0438 Area of the electron tunneling region between the floating gate and the source for resetting the floating gate c
 C_{fc} fF 1089.5358 Capacitance between the floating gate and the control gate
 C_{fsx} fF 0.4059 Capacitance between the floating gate and the silicon substrate
 C_{fd} fF 0.1015 Capacitance between the floating gate and the drain
 C_{fs} fF 0.7103 Capacitance between the floating gate and the source
 C_{fg} fF 1090.7534 Total floating gate capacitance
 $C_{r,w}$ 0.9989 Control gate to floating gate coupling ratio
 $C_{r,src}$ 0.0007 Source junction to floating gate coupling ratio
 $V_{t,fg}$ V 0.90 Threshold voltage of floating gate MOSFET
 V_{erase} 0.00 Erase voltage applied to the source(not used here, set to zero)
 $V_{fg,ini}$ -5.00 Initial floating charged voltage
 V_a 0.00 Actual erase volatge (equal to applied + charge stored on the floating)
 S 4.09E+017 Derived parameter in the floating gate "erase" equation
 X 1.20E+011 Derived parameter in the floating gate "erase" equation

t, sec.	$V_{t,fg}$
0.00001	5.907
2	5.907
4	5.907
8	5.907
16	5.907
32	5.907
64	5.907
128	5.907
256	5.907
512	5.907
1024	5.907
2048	5.907
4096	5.907
8192	5.907
16384	5.907
32768	5.907
65536	5.907
131072	5.907
262144	5.907
524288	5.907
1000000	5.907
2000000	5.907
4000000	5.906
8000000	5.906
1.6E+007	5.906
3.2E+007	5.905
6.4E+007	5.904
.....	5.902
.....	5.898
.....	5.889
.....	5.874



Figures 1I-1J

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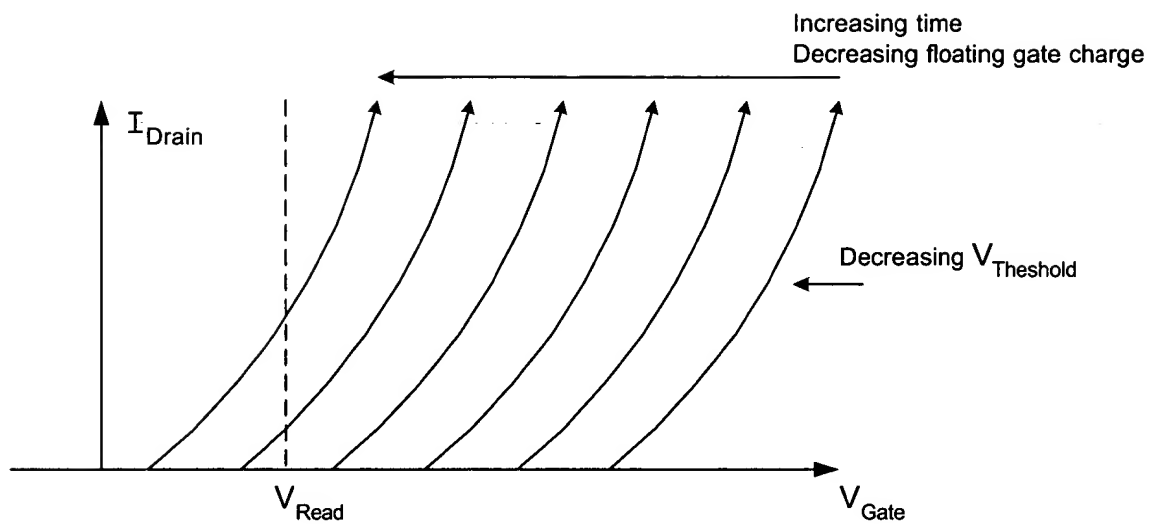


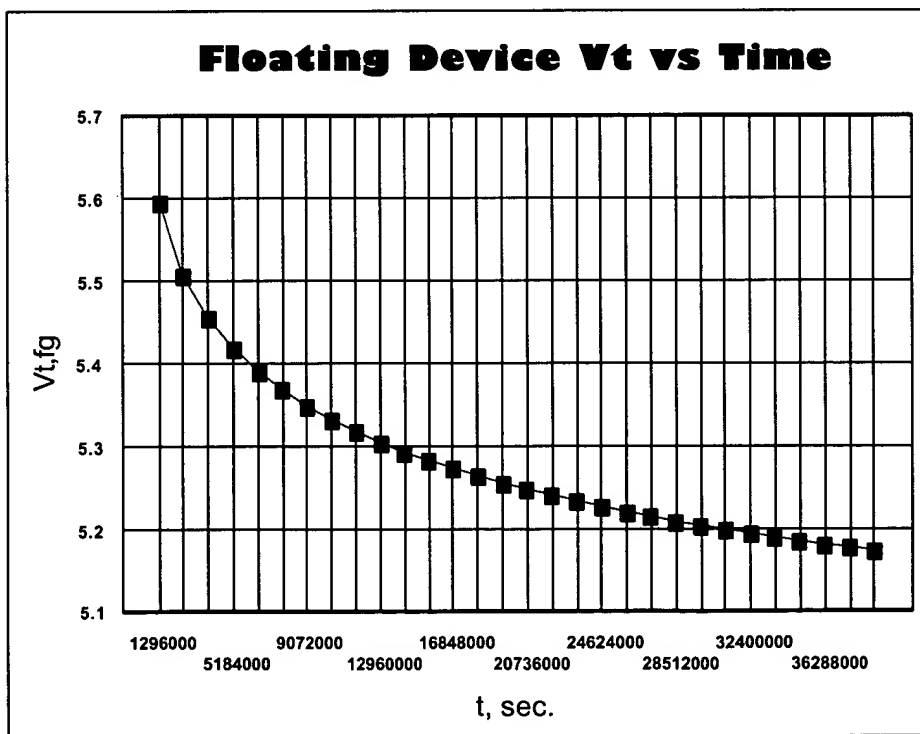
Figure 1K

Calculation of time cell retention characteristics

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	2592000	1 month
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	*****	5184000	2 months
					7776000	3 months
b0, eV (barrier)el	mr, effective mass ratio	T, K degree			*****	4 months
2.9	3.9	0.5	300		*****	5 months
					*****	6 months
C	b				*****	7 months
1.0630E-006	2.3854E+008				*****	8 months
					*****	9 months
					*****	10 months
					*****	11 months
					*****	12 months
					*****	13 months
					*****	14 months
					*****	15 months
					*****	16 months

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	65	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1327	Capacitance between the floating gate and the drain
Cfs fF	0.9288	Capacitance between the floating gate and the source
Cfg fF	1091.1281	Total floating gate capacitance
Cr,wl	0.9985	Control gate to floating gate coupling ratio
Cr,src	0.0009	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating charged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	2.93E+013	Derived parameter in the floating gate "erase" equation
X	1.56E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.909
1296000	5.596
2592000	5.508
3888000	5.456
5184000	5.420
6480000	5.392
7776000	5.369
9072000	5.349
*****	5.333
*****	5.318
1.3E+007	5.305
*****	5.293
*****	5.283
*****	5.273
*****	5.264
*****	5.256
*****	5.248
2.2E+007	5.240
*****	5.234
*****	5.227
*****	5.221
*****	5.215
*****	5.210
*****	5.204
*****	5.199
*****	5.195
*****	5.190
3.5E+007	5.185
*****	5.181
*****	5.177
*****	5.173



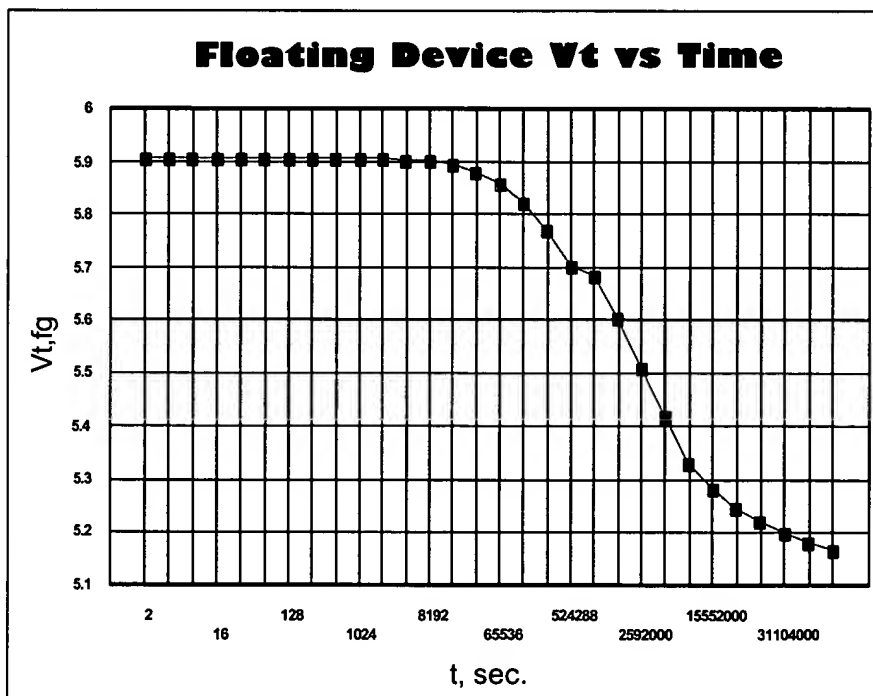
Figures 1L-1M

Calculation of floating cell retention characteristics

					Seconds	Time Periods
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.054588E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	el	mr, effective mass ratio	T, K degree		604800	1 week
2.9	3.9	0.5	300		1209600	2 weeks
					2592000	1 month
C	b				5184000	2 months
1.0630E-006	2.3854E+008				10368000	4 months
					15552000	6 months
					20736000	8 months
					25920000	10 months
					31104000	12 months
					36288000	14 months
					41472000	16 months

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	65	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1327	Capacitance between the floating gate and the drain
Cfs fF	0.9288	Capacitance between the floating gate and the source
Cfg fF	1091.1281	Total floating gate capacitance
Cr,wl	0.9985	Control gate to floating gate coupling ratio
Cr,src	0.0009	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating charged voltage
Va	0.00	Actual erase voltage (equal to applied + charge stored on the floating)
S	2.93E+013	Derived parameter in the floating gate "erase" equation
X	1.56E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.909
2	5.909
4	5.909
8	5.909
16	5.909
32	5.909
64	5.909
128	5.909
256	5.908
512	5.908
1024	5.908
2048	5.907
4096	5.905
8192	5.902
16384	5.895
32768	5.883
65536	5.861
131072	5.824
262144	5.771
524288	5.702
1048576	5.686
2097152	5.604
4194304	5.508
8388608	5.420
16777216	5.333
33554432	5.283
67108864	5.248
134217728	5.221
268435456	5.199
536870912	5.181
1073741824	5.166



Figures 1N-10

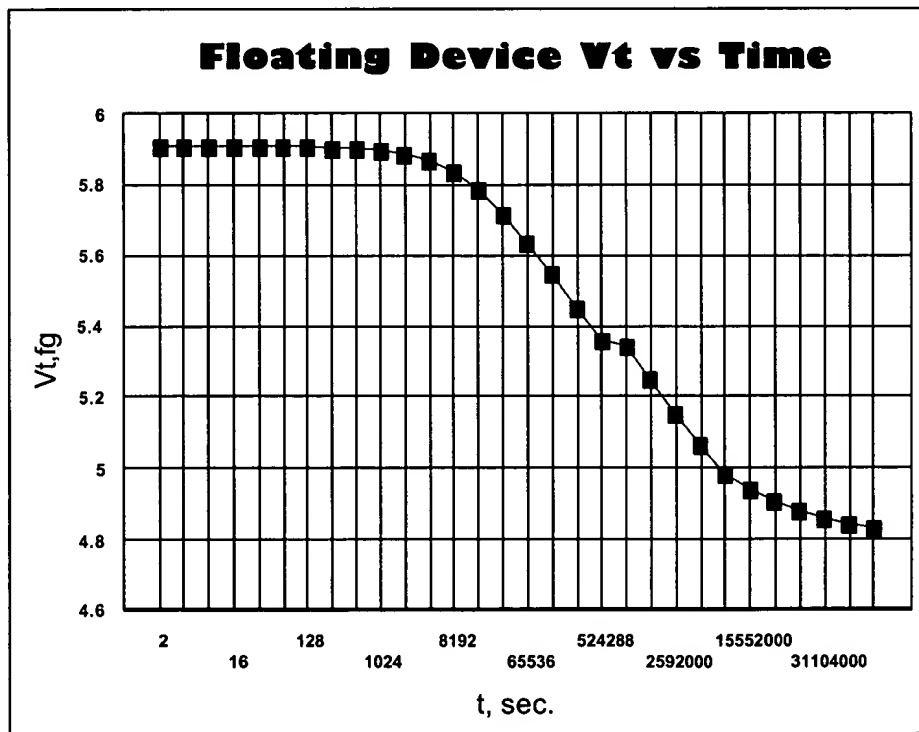
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Calculation of floating cell retention characteristics

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	3600	1 hour
					86400	1 day
b0, eV (barrier)	el	mr, effective mass ratio	T, K degree		604800	1 week
2.9		3.9	0.5	300	1209600	2 weeks
					2592000	1 month
C	b				5184000	2 months
1.0630E-006	2.3854E+008				4 months
					6 months
					8 months
					10 months
					12 months
					14 months
					16 months

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	60	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um ²	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx fF	0.5750	Capacitance between the floating gate and the silicon substrate
Cfd fF	0.1438	Capacitance between the floating gate and the drain
Cfs fF	1.0063	Capacitance between the floating gate and the source
Cfg fF	1091.2608	Total floating gate capacitance
Cr,wl	0.9984	Control gate to floating gate coupling ratio
Cr,src	0.0009	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating charged voltage
Va	0.00	Actual erase volatge (equal to applied + charge stored on the floating)
S	2.70E+012	Derived parameter in the floating gate "erase" equation
X	1.69E+011	Derived parameter in the floating gate "erase" equation

t, sec.	Vt,fg
0.00001	5.909
2	5.909
4	5.909
8	5.909
16	5.909
32	5.909
64	5.909
128	5.908
256	5.907
512	5.904
1024	5.898
2048	5.888
4096	5.870
8192	5.838
16384	5.789
32768	5.721
65536	5.639
131072	5.549
262144	5.455
524288	5.360
1048576	5.341
2097152	5.250
4194304	5.152
8388608	5.067
16777216	4.985
33554432	4.938
67108864	4.906
134217728	4.881
268435456	4.861
536870912	4.844
1073741824	4.830



Figures 1P-1Q

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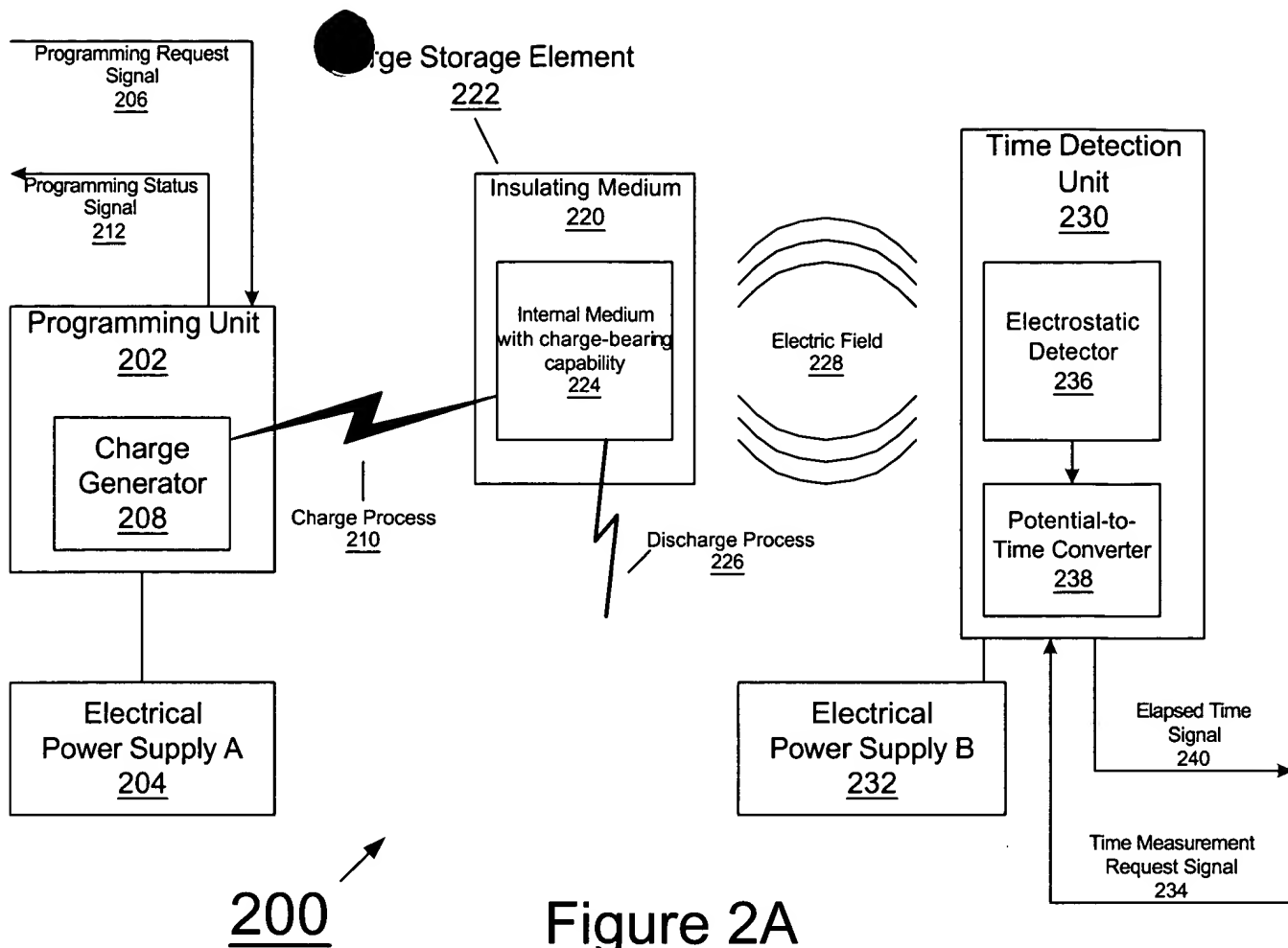


Figure 2A

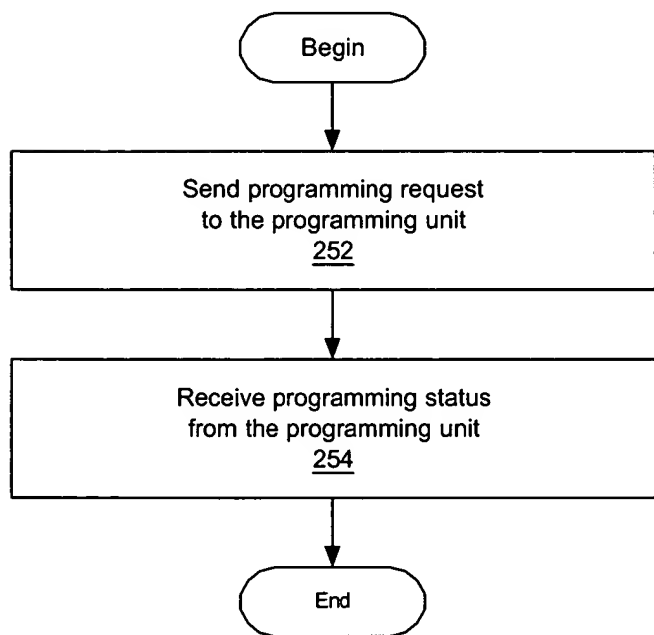


Figure 2B

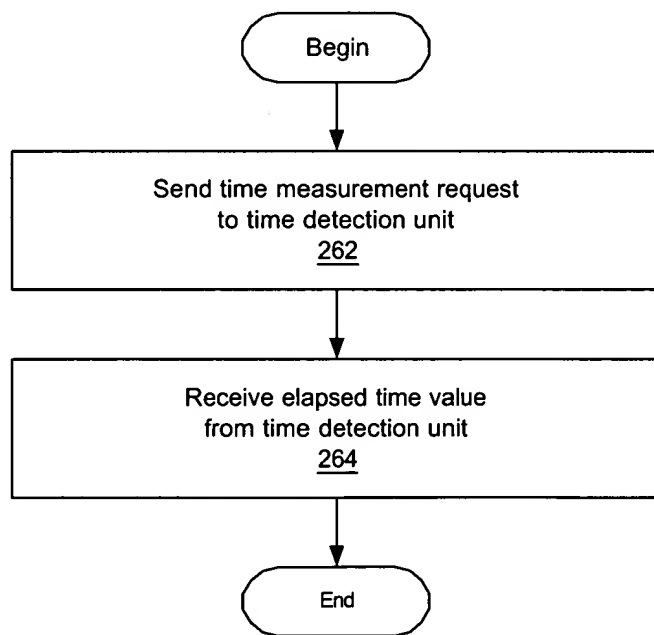


Figure 2C

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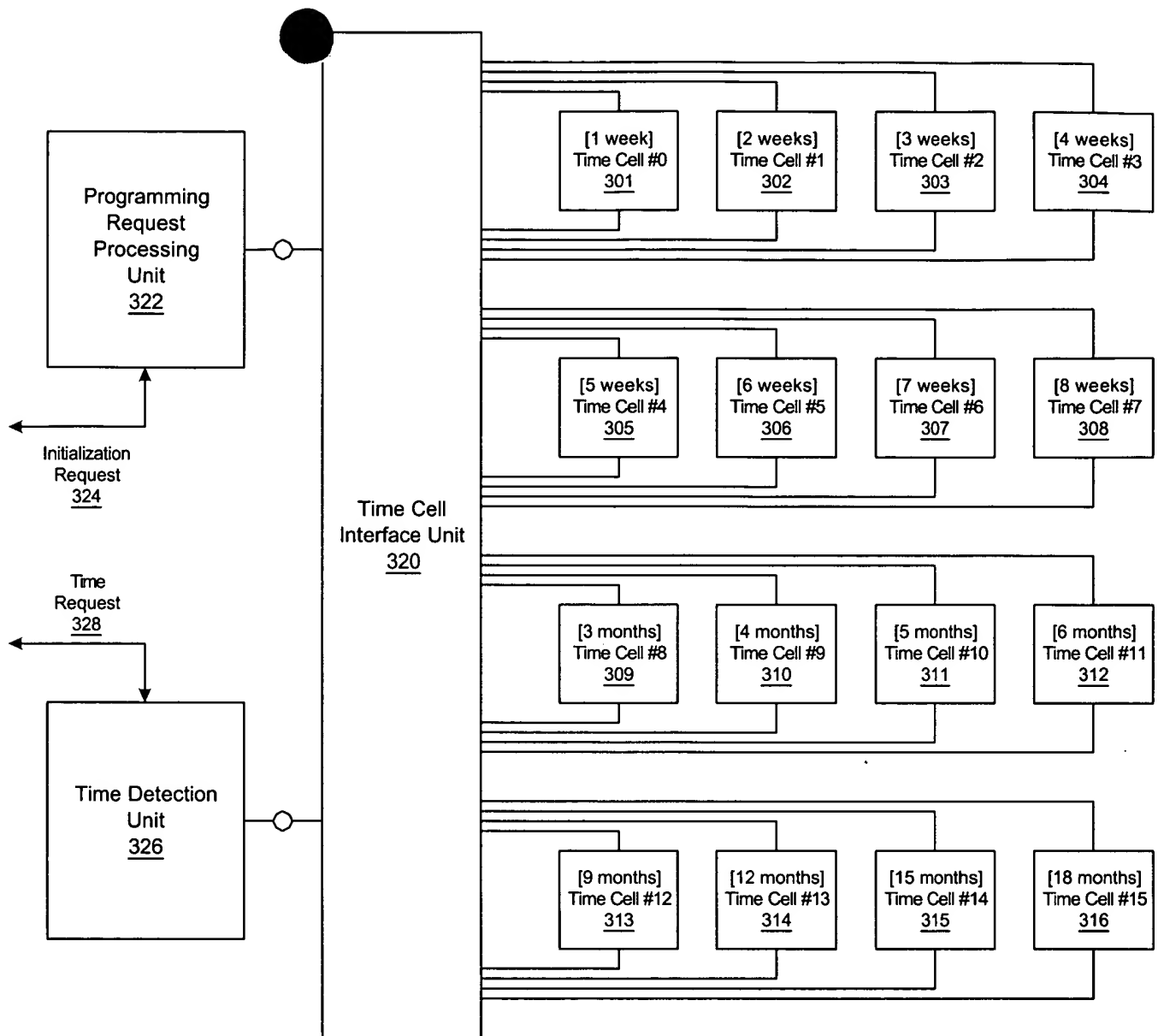


Figure 3A

The diagram illustrates the internal structure of the Time Cell Interface Unit 330. It features a central vertical bus with two connection points (circles) on the left. The unit is divided into four horizontal sections, each containing a set of time cells. The top section is connected to the upper bus point and contains four time cells: [1 week] Time Cell #0 331, [2 weeks] Time Cell #1 332, [3 weeks] Time Cell #2 333, and [4 weeks] Time Cell #3 334. The second section contains four time cells: [1 week] Time Cell #4 335, [2 weeks] Time Cell #5 336, [3 weeks] Time Cell #6 337, and [4 weeks] Time Cell #7 338. The third section is connected to the lower bus point and contains four time cells: [2 months] Time Cell #8 339, [4 months] Time Cell #9 340, [6 months] Time Cell #10 341, and [8 months] Time Cell #11 342. The bottom section contains four time cells: [2 months] Time Cell #12 343, [4 months] Time Cell #13 344, [6 months] Time Cell #14 345, and [8 months] Time Cell #15 346. A Time Set Identifier Unit 348 is connected to the top of the unit, and a Time Cell Interface Unit 330 is connected to the bottom of the unit.

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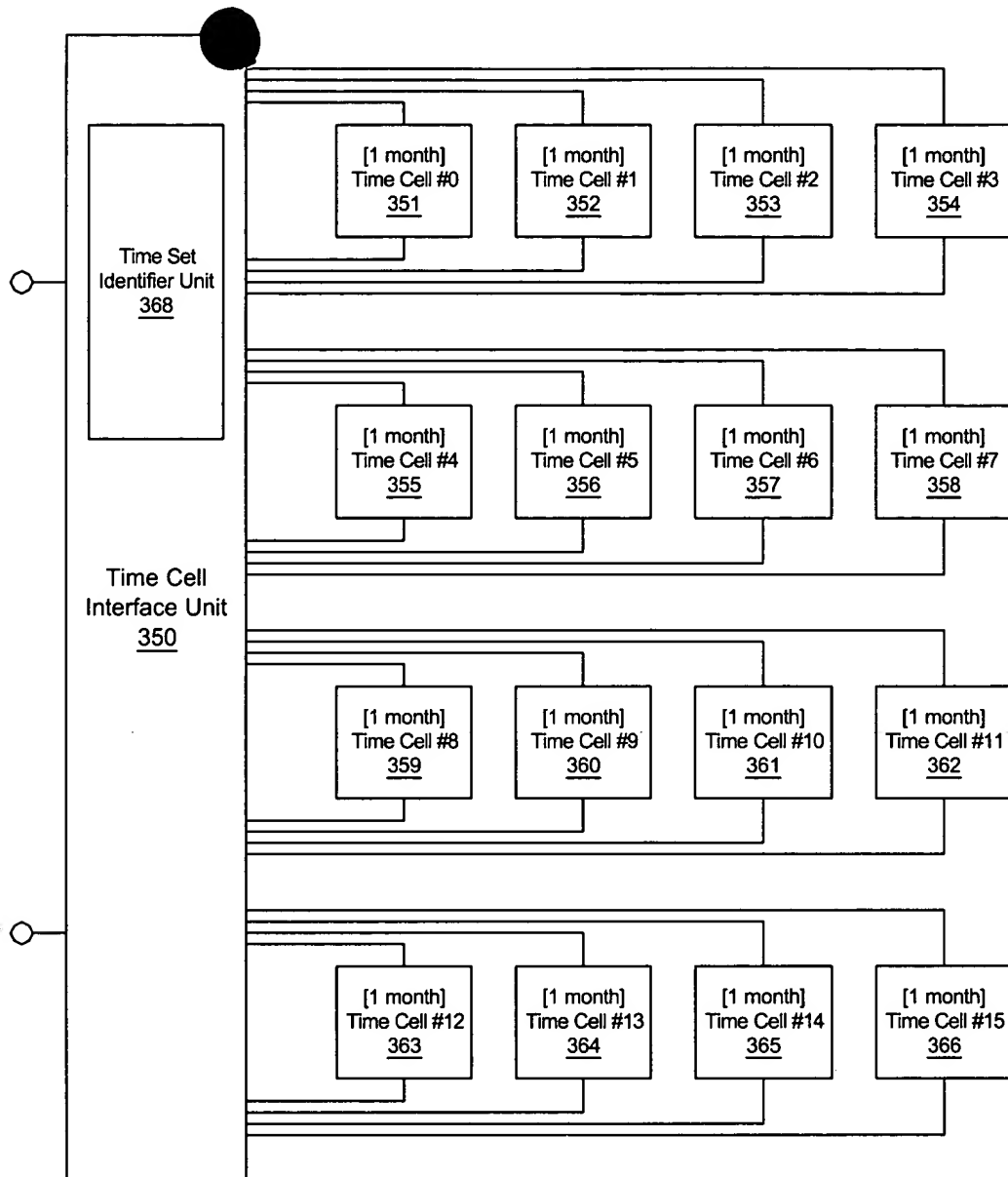


Figure 3C

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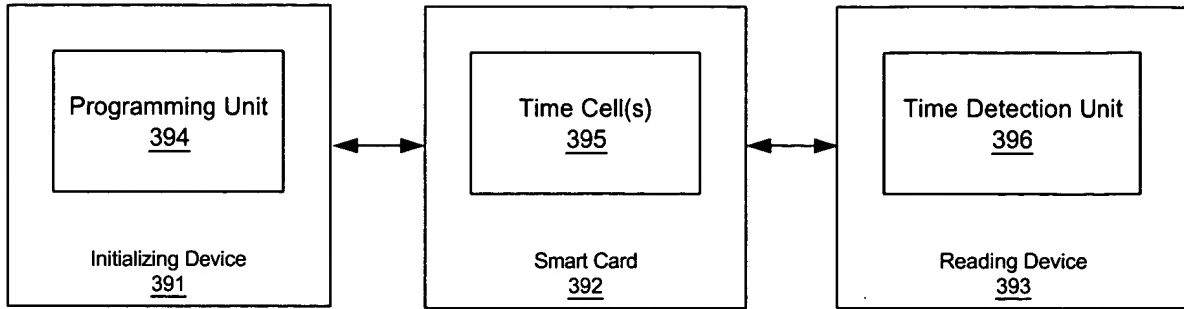


Figure 3F

00T EOT" 44E0260

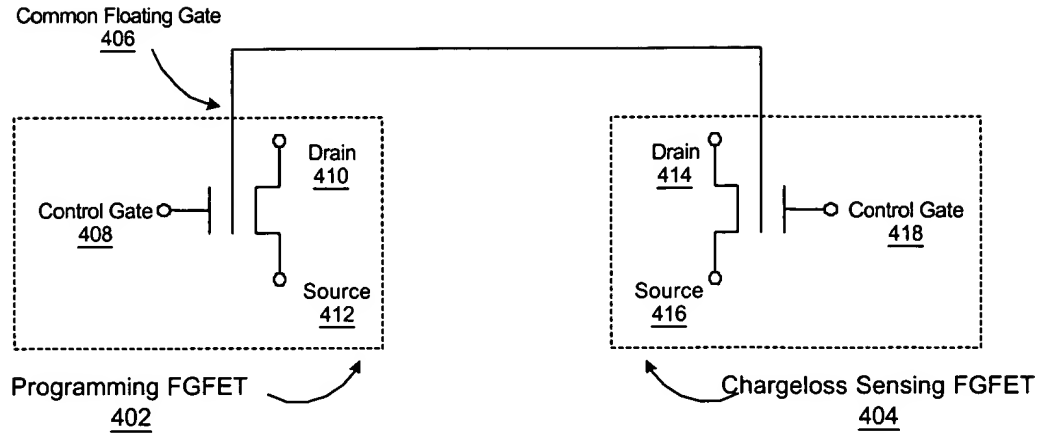


Figure 4A

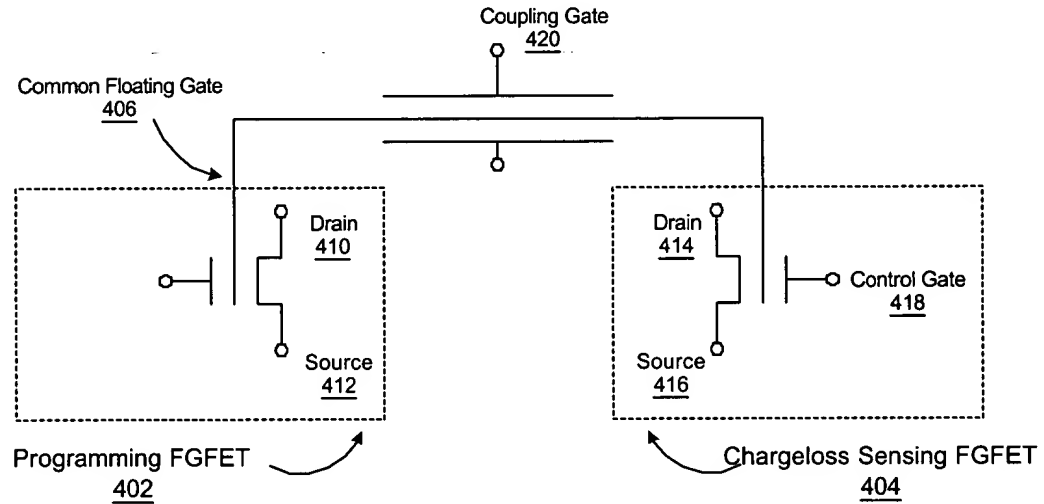


Figure 4B

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Voltages during programming operation

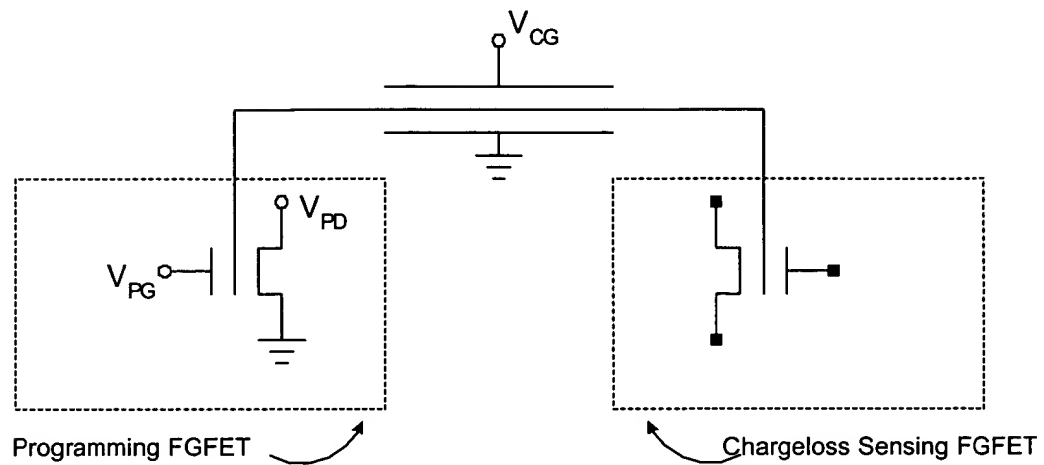


Figure 4C

Voltages during sensing operation

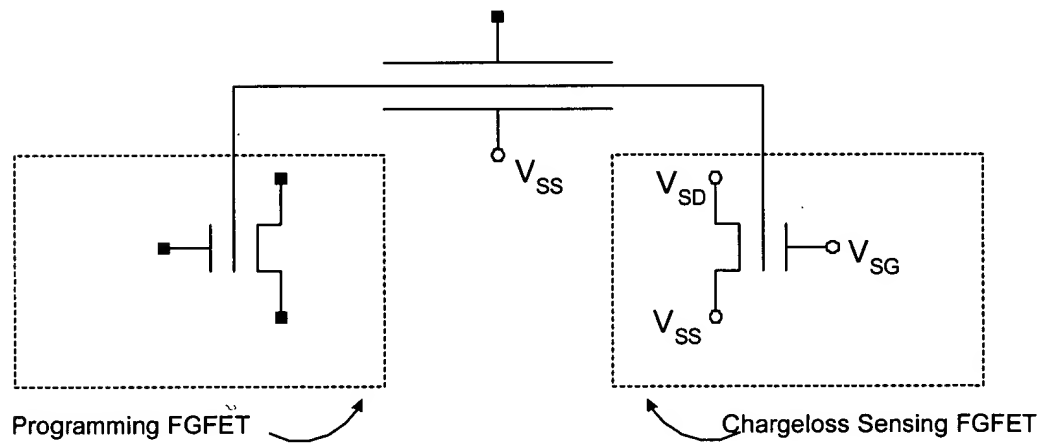
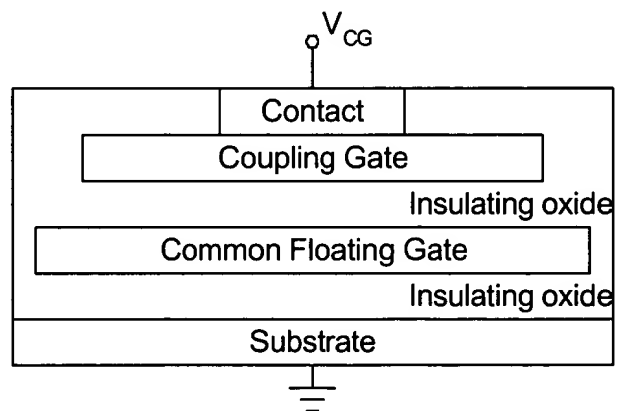


Figure 4D

The diagram illustrates a 1T1C1F1S1P1 architecture. It features a central 'Common Floating Gate' (FG) and a 'Coupling' region. On the left, a 'Programming FGFET' is shown with its gate connected to V_{PG} and its source to Ground. On the right, a 'Chargeless Sensing FGFET' is shown with its gate connected to V_{SG} and its source to V_{SS} . The central FG is connected to V_{PD} and V_{SD} . The coupling region is connected to V_{CG} . The diagram also shows a 'Common Floating Gate' and a 'Coupling' region.



The diagram illustrates a differential pair circuit for charge loss sensing. It features two resistors, R_1 and R_2 , connected to a common V_{DD} supply. The gates of the two FETs are connected to a differential pair of nodes, V_1 and V_2 , which are also connected to the drains of the FETs. The source of the FET connected to V_1 is connected to ground through a "Detector FET". The source of the FET connected to V_2 is connected to ground through a "Charge Loss Sensing FGFET". The gates of these two FETs are connected to a common node, V_{SG} . The drains of these two FETs are connected to a common node, V_{SD} . The output of the differential pair is V_{OUT} , which is connected to the gates of the two FETs. The circuit is powered by V_{DD} and ground.

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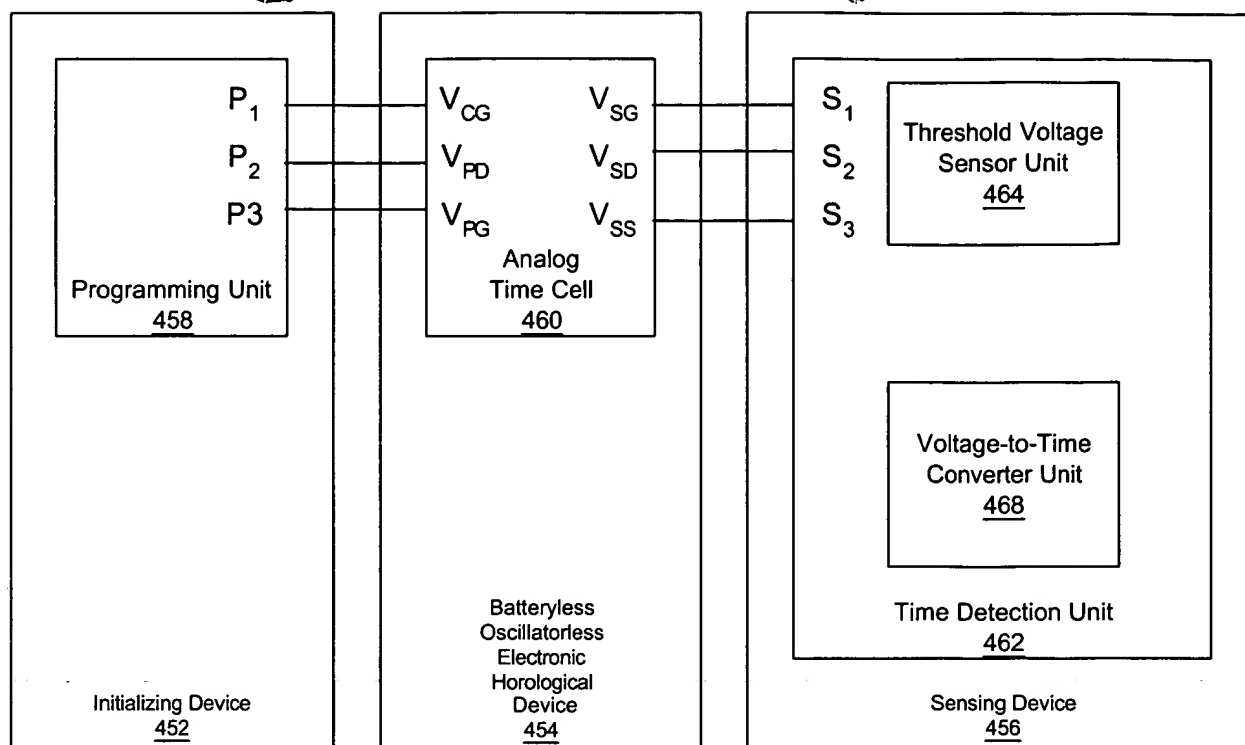


Figure 4K

470

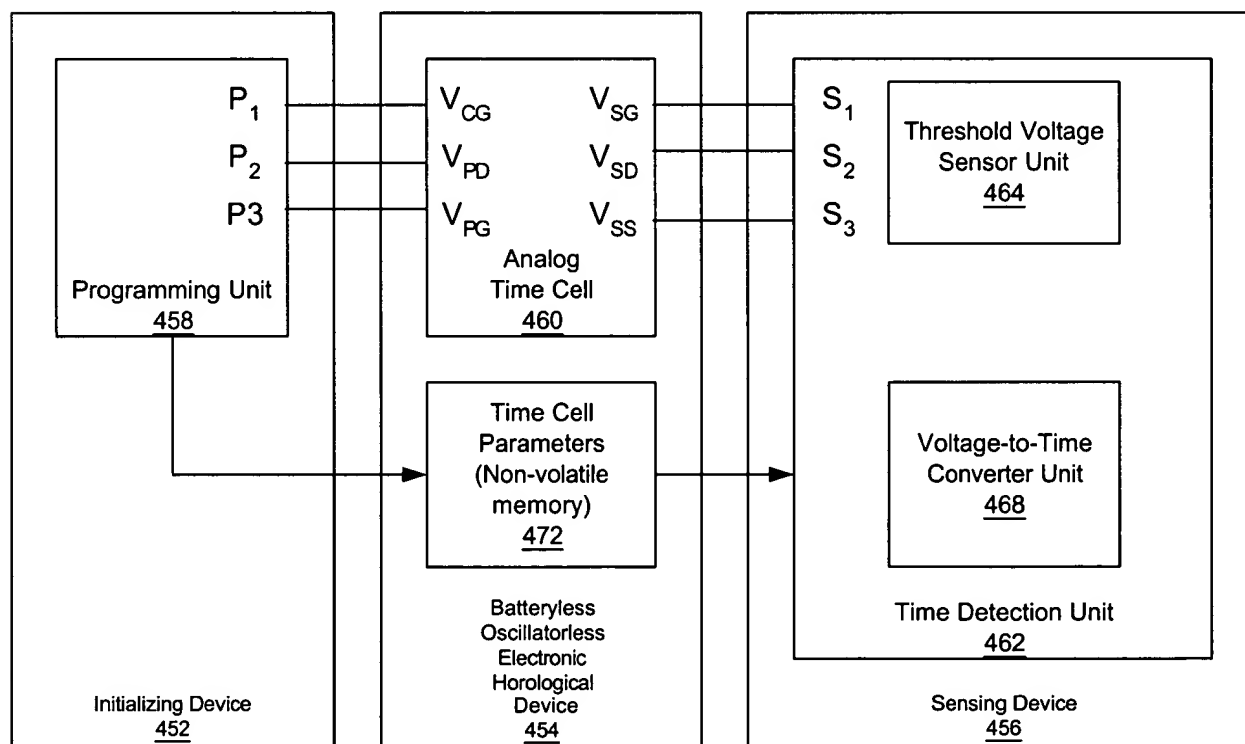


Figure 4L

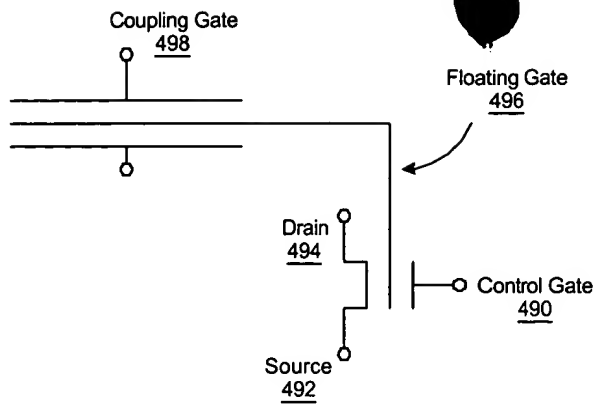


Figure 4M

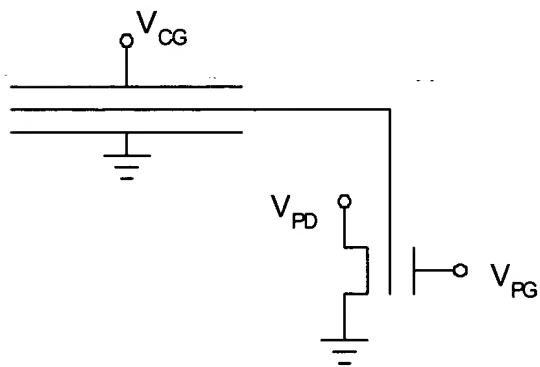


Figure 4N

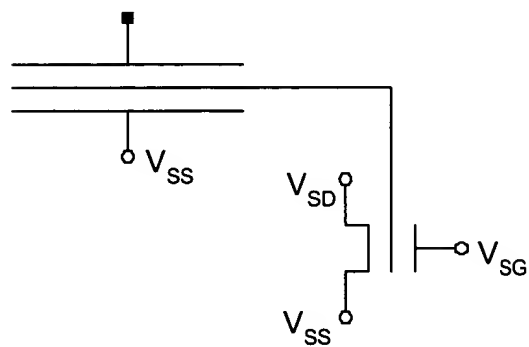


Figure 4O

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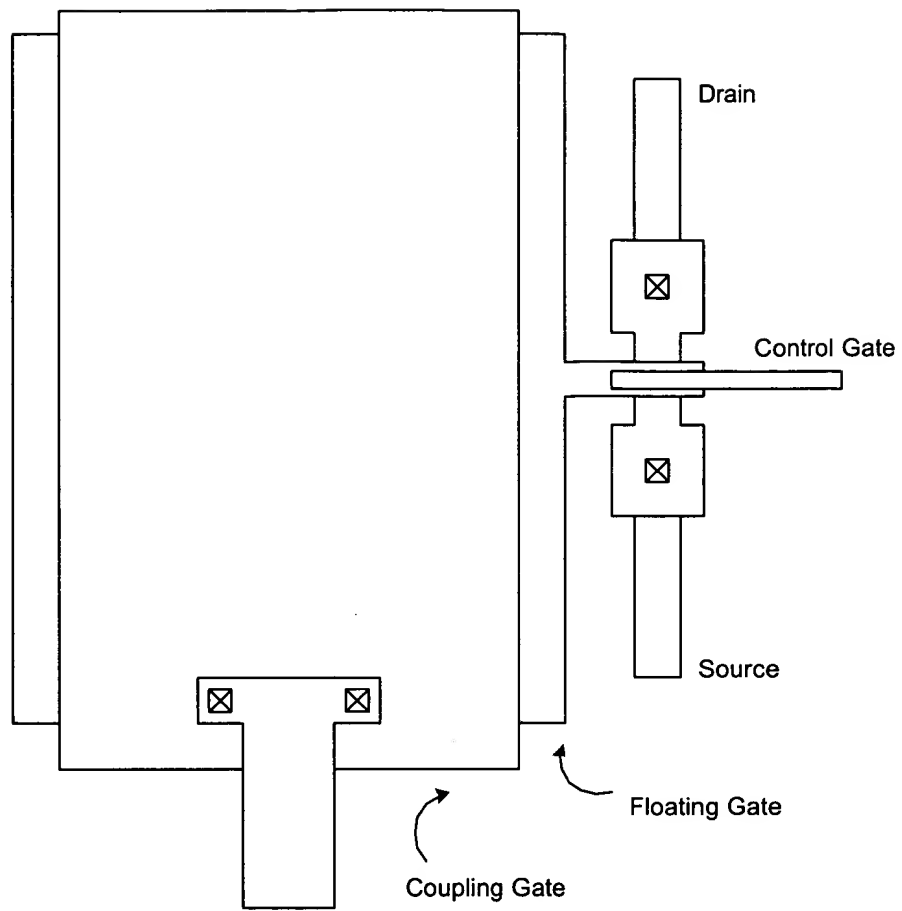


Figure 4P